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Design Review II

Designing an Efficient Sub-threshold FPGA Switchbox

**Progress**

We have made some progress in our exploration of the FPGA interconnect, both analytically and through simulation. In terms of the analytical progress, we have been able to use a mathematical model to calculate the current and delay through each of the three switchbox structures (tri-state inverter, transmission gate, and pass gate) that we intend on testing. The constants for the calculations were extracted from TASE simulations and from model files in the TASE database, which are attached. We have calculated the delays in the two ways we have discussed in class – using the average resistance method and using the average current method. We think that for our exploration the average resistance method makes more sense. First, this allows for simple Elmore Delay calculations, as the avg. R is already calculated. It is also demonstrated that the avg. R method is a more conservative (higher delay) approach to calculations, which is better for us as designers.

In terms of simulation data, we have had our share of troubles. We were able to create ideal switch architectures using TASE, which allows the user to repeat the simulations for any technology node (feature size). We also simulated the same results using a buffered input as opposed to an idealized input. To buffer the inputs, we ran an ideal input signal through an inverter, and then made sure the net that included the output of that inverter had a fanout of 4. This provided a realistic input signal for our plots, and it of course added delay. In addition to buffering the inputs, the simulations are expanding to paths which include multiple switches – up to 10. So far, only tri-state buffers have been successfully simulated, and we find now that those are not affected by Elmore delay (explanation on figure).

**Remaining Tasks**

There is quite a bit of work left to be done on this project. The overall goal is to be able to both analytically and through simulation test different interconnect topologies, in different interconnect scenarios, and find their best applications. To do this, we will need to create simulations where the switches are in a single path, as well as one with them in a branching path (particularly in sub-vt). To really look at the efficiency of a technology in the way we would like to, we also need to get Power (and thus energy) information from the simulations. Power and energy are especially important because we will need those to develop Pareto curves, which are good graphics for illustrating the comparisons we plan on making in the future.

The structure of the simulation needs to be more reflective of a true FPGA interconnect. This includes the additional load that is seen on the FPGA interconnect. When any signal hits a switch box, there are at least two (in the case of a pass gate interconnect) other switches hanging off of that path. We have attempted to expand the simulations to paths, and to include the extra switches along the paths, but we have had trouble getting those simulations to run. Once each simulation is built, it shouldn’t be too difficult to get all of the simulation data (Power, Delay, Area, etc.) from them.

**Challenges**

This project has proven to be more challenging than we expected. Simulation has been our biggest challenge in terms of potentially preventing progress. For one, our simulating tools and their syntax were foreign to both of us, and we are still working to understand them better. Secondly, our understanding of propagation delay and power dissipation for these structures isn’t quite an expertise yet, but we are working towards that level of knowledge.

There is a much more specific simulation challenge. It seems to us that in Sub-Vt, the voltage swing for pass gates in series diminishes to the point that the propagation delay for the simulation cannot be calculated in the manner we calculated it for just one pass gate. There is a possibility that it may work with paths that are smaller than 10, but we are still in the process of testing and creating these different interconnect scenarios.

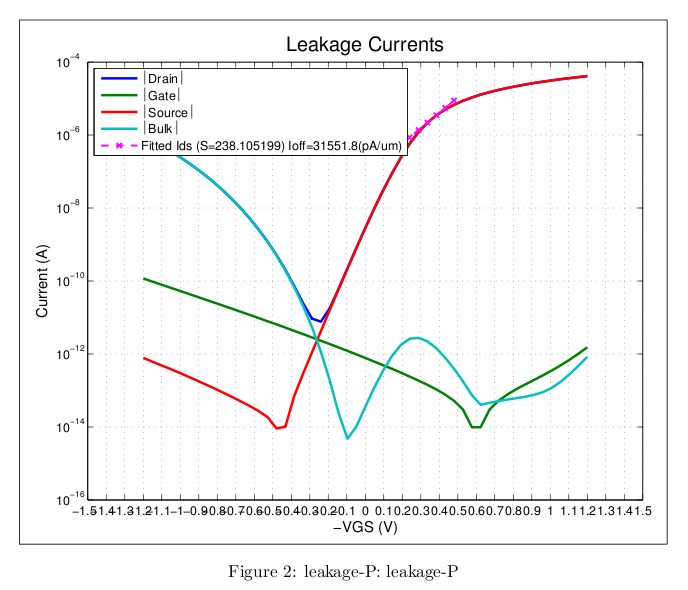
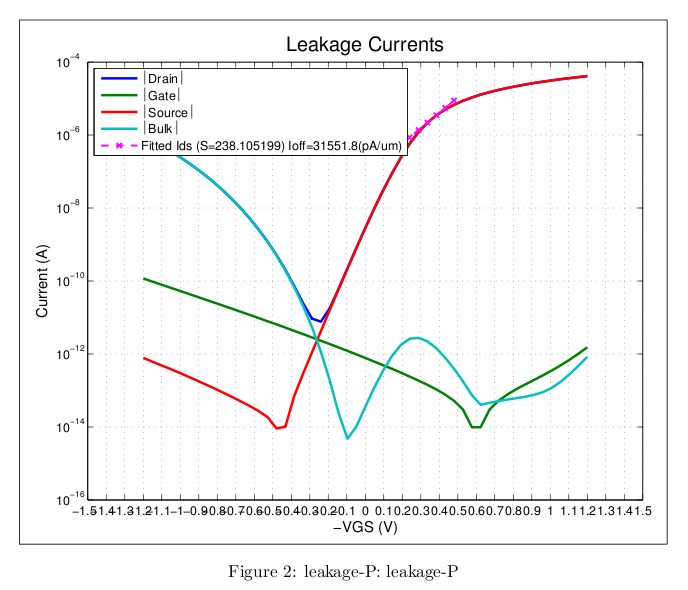
**Timeline**

We honestly have failed to meet our timeline. At this point, we should have finished collecting both simulation and analytical data concerning delay and energy for all three structures. We are not quite there yet. The only choice we have as a group is to ramp up the work that we do on the project, so that we can get results as soon as possible.

Example schematic: Buffered Pass Gate Test



The 5 inverters tied in this manner provide a more realistic signal for our simulations.



Above are two TASE tests which extract ‘S’, which we used in our model.



This graph shows the new model for the passgate. The delay model matches the values of the buffered simulation very well. Capacitive Load was calculated using variables in the definition files for the transistors, with a bit of guess-and-check with added capacitance and the I0 term for the current to create the proper fit.



This graph shows the dependence of delay on VDD for a transmission gate.

Concern – S\_n was changed for a passgate to make that model fit, and S\_p was changed make this fit, while keeping S\_n constant. Couldn’t that pose a potential problem? Won’t there be ambiguity as to which metric is off, based on the predictions we try to make from it?



n=5

n=10

This graph shows the different delays for a tri-state inverter for a different number of them in series. Analytics at this point do not take into account wire cap or delay. n = 1 is the bottom-most plot, and they go up through n=10 at the top. Delay should scale as , where n is the number of gates in the path. In other words, the delay for n=10 should be or 55x the delay for n=1. At first glance, this looks like this isn’t the case (22x). There is a discrepancy because the above graph uses the average between tPLH and tPHL. The solely tPHL plot shows that 55x increase that is expected.



This plot shows our model for the average tP (using tPHL and tPLH) of each structure. Since pass gates are not good at pulling L-H (due to diminishing VGS and bulk effect), the tP changes drastically for that structure.



This is simulation for a path of tri-state inverters. Shown is the delay after 2, 4, and 10 switches. With a 5x difference in number of switches, the delay increases by about 5, suggesting that there is a linear dependence on due to the switch boxes, and not an Elmore-type delay. This is because tri-state inverters discharge to ground through themselves, and don’t need another path to go through.